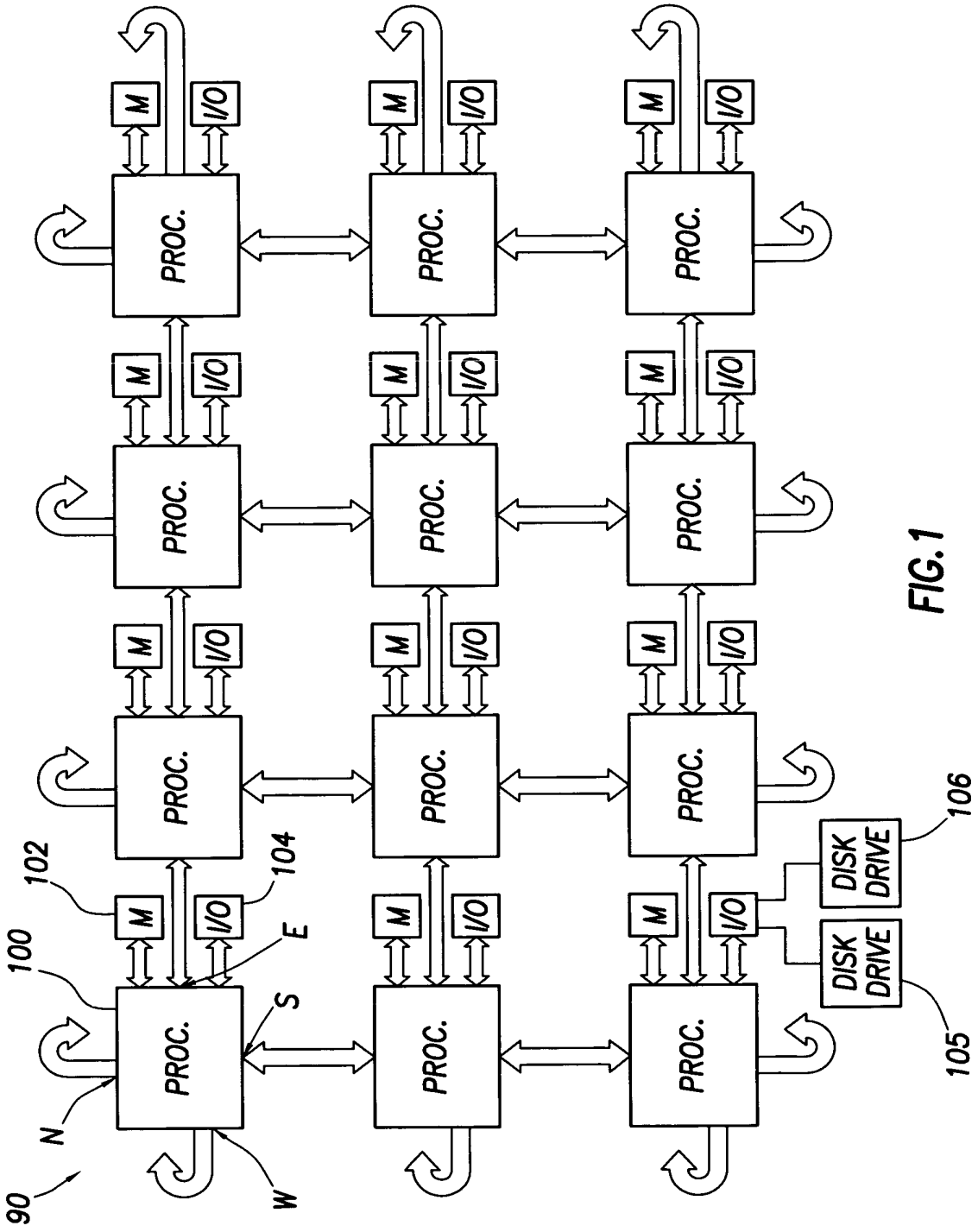


FIG. 1

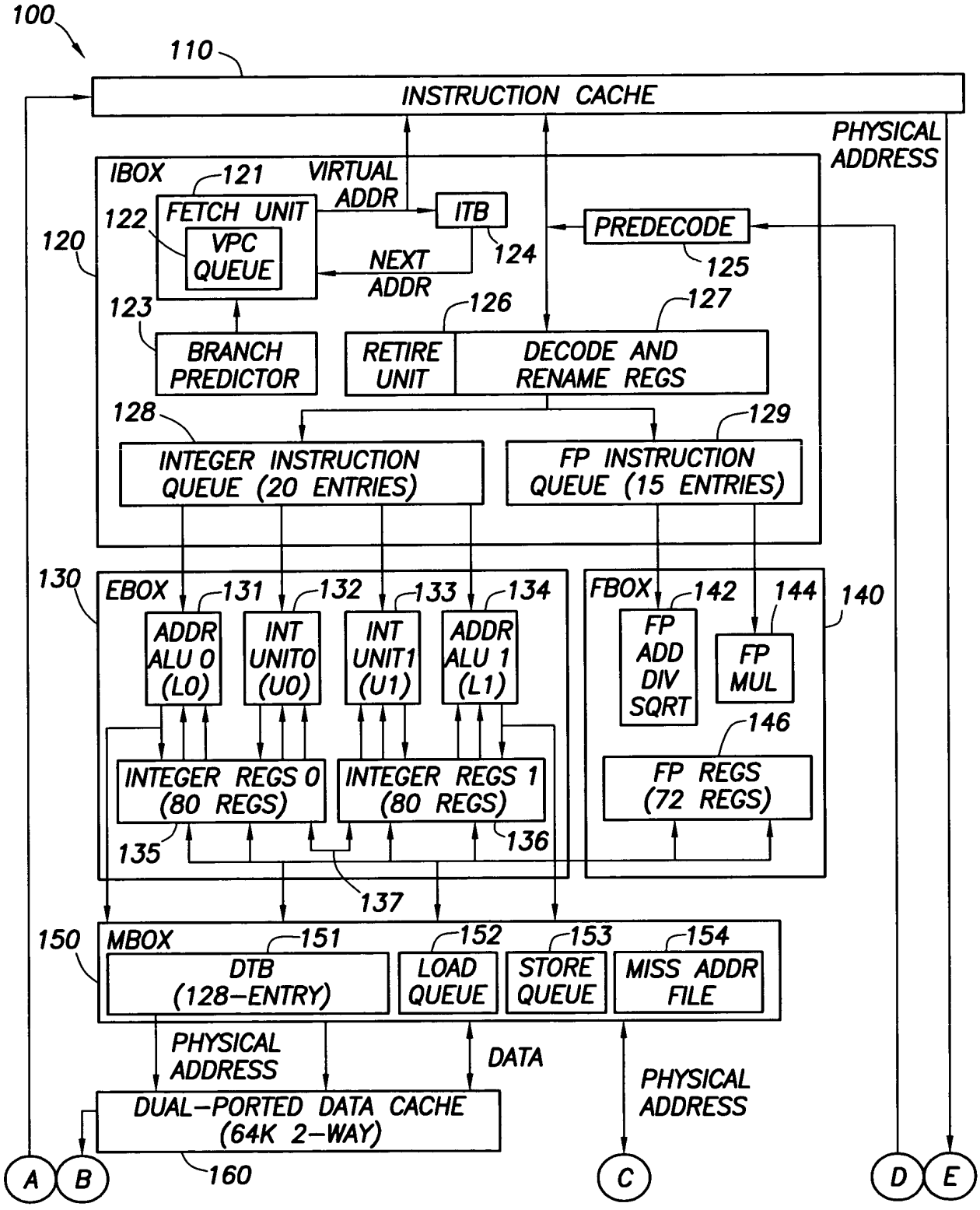

100
110
INSTRUCTION CACHE
PHYSICAL ADDRESS
IBOX
121
VIRTUAL ADDR
FETCH UNIT
122
VPC QUEUE
ITB
124
PREDECODE
125
120
NEXT ADDR
123
126
127
BRANCH PREDICTOR
RETIRE UNIT
DECODE AND RENAME REGS
128
129
INTEGER INSTRUCTION QUEUE (20 ENTRIES)
FP INSTRUCTION QUEUE (15 ENTRIES)
130
EBOX
131
132
133
134
FBOX
142
144
140
ADDR ALU 0 (L0)
INT UNIT0 (U0)
INT UNIT1 (U1)
ADDR ALU 1 (L1)
FP ADD DIV SQRT
FP MUL
146
INTEGER REGS 0 (80 REGS)
INTEGER REGS 1 (80 REGS)
FP REGS (72 REGS)
135
136
137
150
MBOX
151
152
153
154
DTB (128-ENTRY)
LOAD QUEUE
STORE QUEUE
MISS ADDR FILE
PHYSICAL ADDRESS
DATA
PHYSICAL ADDRESS
DUAL-PORTED DATA CACHE (64K 2-WAY)
160
A
B
C
D
E

FIG.2a

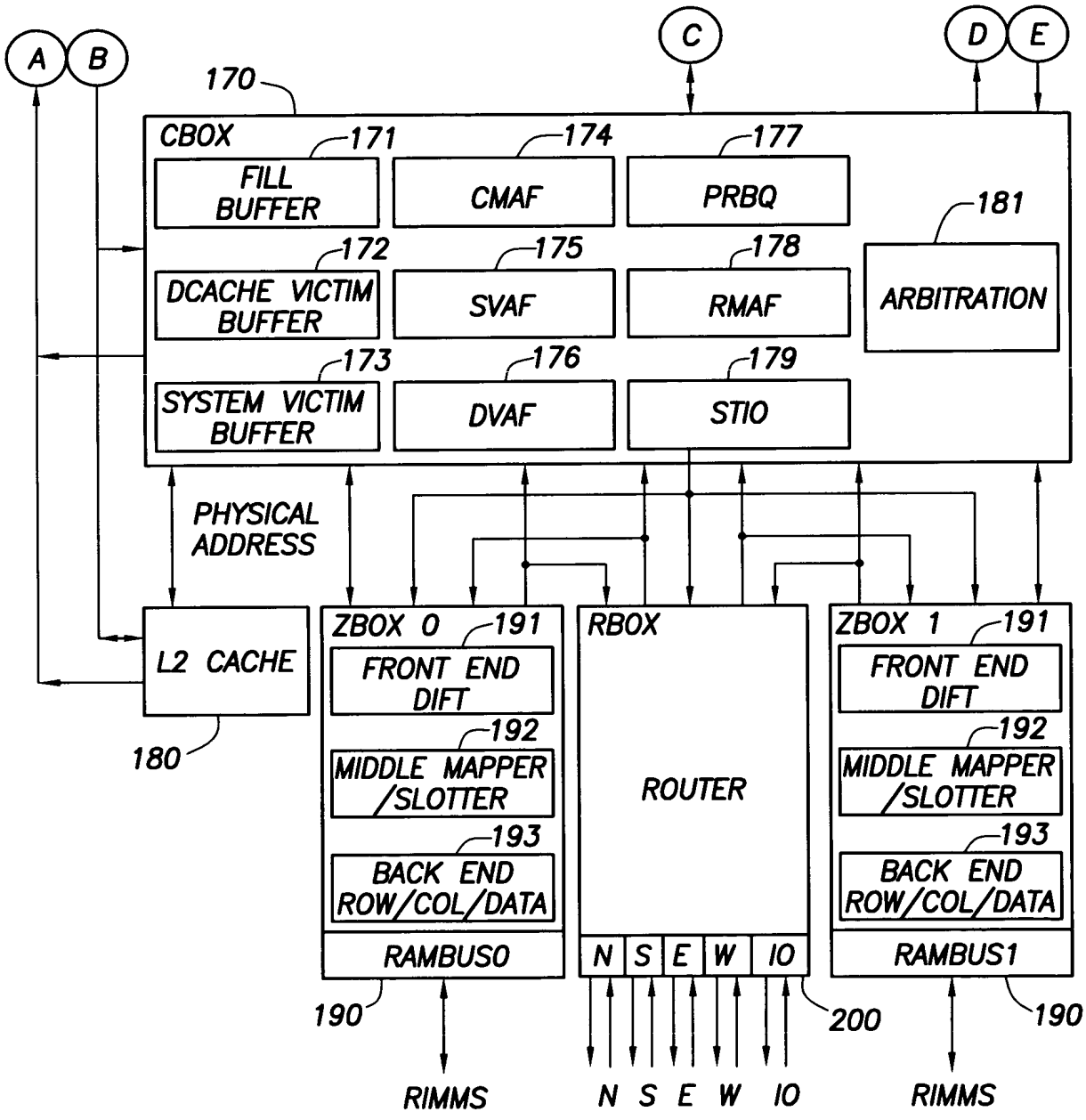

A
B
C
D
E
170
CBOX
171
FILL BUFFER
174
CMAF
177
PRBQ
181
ARBITRATION
172
DCACHE VICTIM BUFFER
175
SVAF
178
RMAF
173
SYSTEM VICTIM BUFFER
176
DVAF
179
STIO
PHYSICAL ADDRESS
L2 CACHE
180
ZBOX 0
191
FRONT END DIFT
192
MIDDLE MAPPER /SLOTTER
193
BACK END ROW/COL/DATA
RAMBUS0
190
RIMMS
RBOX
ROUTER
N
S
E
W
IO
200
N S E W IO
ZBOX 1
191
FRONT END DIFT
192
MIDDLE MAPPER /SLOTTER
193
BACK END ROW/COL/DATA
RAMBUS1
190
RIMMS

FIG.2b

FIG.3

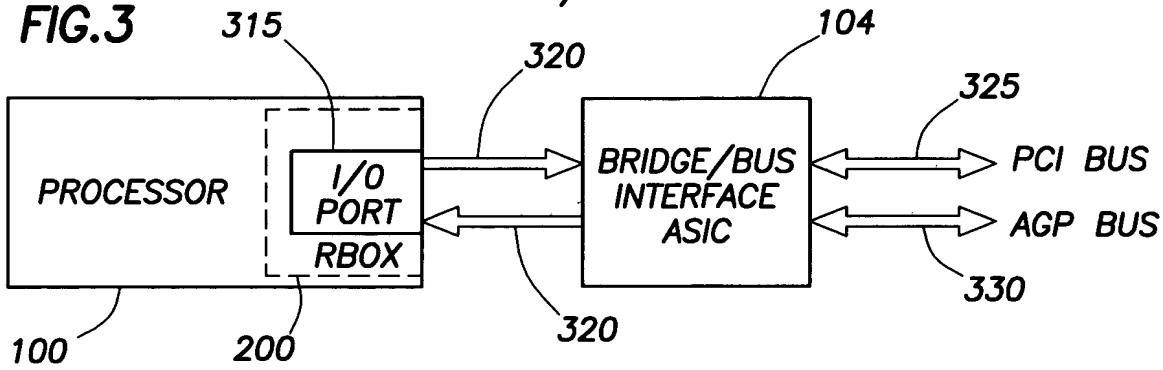
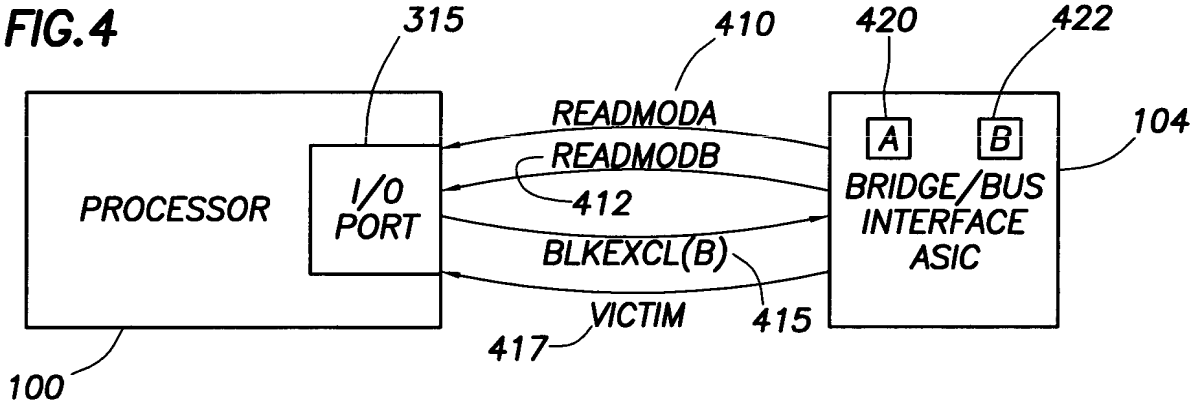


FIG.4



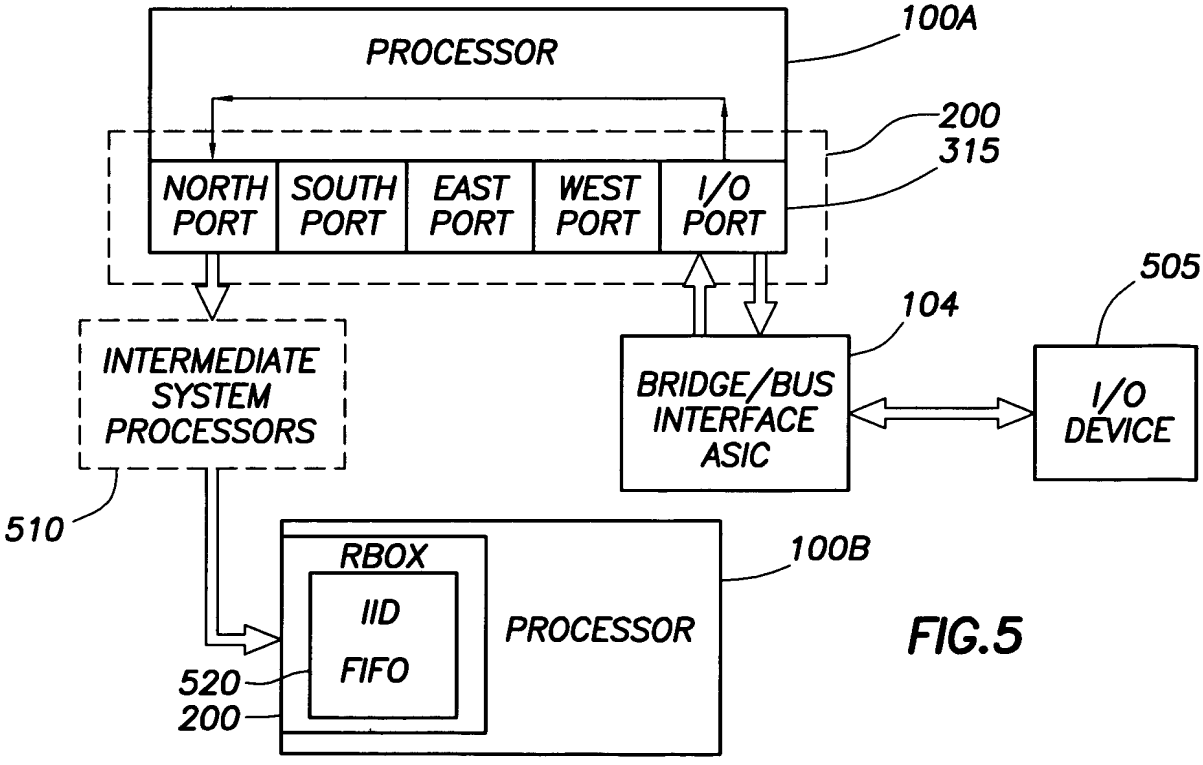


FIG.5